AF/2823 #
IFW

DOCKET NO. 91-C-127C1 (STMI01-00022) **PATENT**
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	Jia Li
U.S. Serial No.	:	09/803,715
Filed	:	March 9, 2001
For	:	METHOD OF FORMING ACTIVE AND ISOLATION AREAS WITH SPLIT ACTIVE PATTERNING
Group No.	:	2823
Examiner	:	Julio J. Maldonado

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
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Sir:

The undersigned hereby certifies that the following documents:

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2. Check in the amount of $330.00 for the Appeal Brief filing fee;
3. Fee Transmittal for FY 2004 (in duplicate); and
4. Postcard receipt;

relating to the above application, were deposited as "First Class Mail" with the United States Postal Service, addressed to MAIL STOP APPEAL BRIEF - PATENTS, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on June 8, 2004 .

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FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 330.00

Complete if Known	
Application Number	09/803,715
Filing Date	March 9, 2001
First Named Inventor	Jia Li
Examiner Name	Julio J. Maldonado
Art Unit	2823
Attorney Docket No.	91-C-127C1 (STMI01-00022)

METHOD OF PAYMENT *(check all that apply)*

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Deposit Account Name: 50-0208

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) -0-

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below	Fee Paid
Total Claims		-20** =		X	=
Independent Claims		- 3** =		X	=
Multiple Dependent					=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) -0-

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330.00
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 330.00

SUBMITTED BY				(Complete *(if applicable)*)	
Name (Print/Type)	Daniel E. Venglarik	*Registration No. (Attorney/Agent)*	39,409	*Telephone*	972-628-3600
Signature				*Date*	June 8, 2004

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DOCKET NO. 91-C-127C1 (STMI01-00022) PATENT
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Group No.	:	2823
Examiner	:	Julio J. Maldonado

BOX AF
Commissioner for Patents
Washington, D. C. 20231

Sir:

APPELLANT'S BRIEF ON APPEAL

This Brief is submitted in triplicate on behalf of Appellant for the application identified above. A check is enclosed for the $330.00 fee for filing a Brief on Appeal. Please charge any additional necessary fees to Deposit Account No. 50-0208.

06/15/2004 AWONDAF1 00000096 09803715
01 FC:1402 330.00 OP

REAL PARTY IN INTEREST

The real party in interest for this appeal is the assignee of the application, STMICRO-ELECTRONICS, INC. (f/k/a SGS-THOMSON MICROELECTRONICS, INC.).

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences related to the present application which are currently pending.

SUMMARY OF THE INVENTION

The specification as filed notes the difficulty, with conventional processes, of mask allocation in forming isolation oxides with channel stop implants thereunder between active areas for a silicon substrate, where such conventional processes typically requiring three masks (and associated patterning steps) preventing optimization of critical dimension. Specification, page 3, lines 1–17. To address that problem regarding critical dimension (and mask allocation), the invention employs only two patterning steps to both pattern the oxidation barrier defining the isolation regions and active areas as well as the channel stop implants. Specification, page 4, lines 2–21.

In the present invention, an oxidation barrier 110 of nitride over a pad oxide is formed over a substrate having an n region 102 and a p region 104:

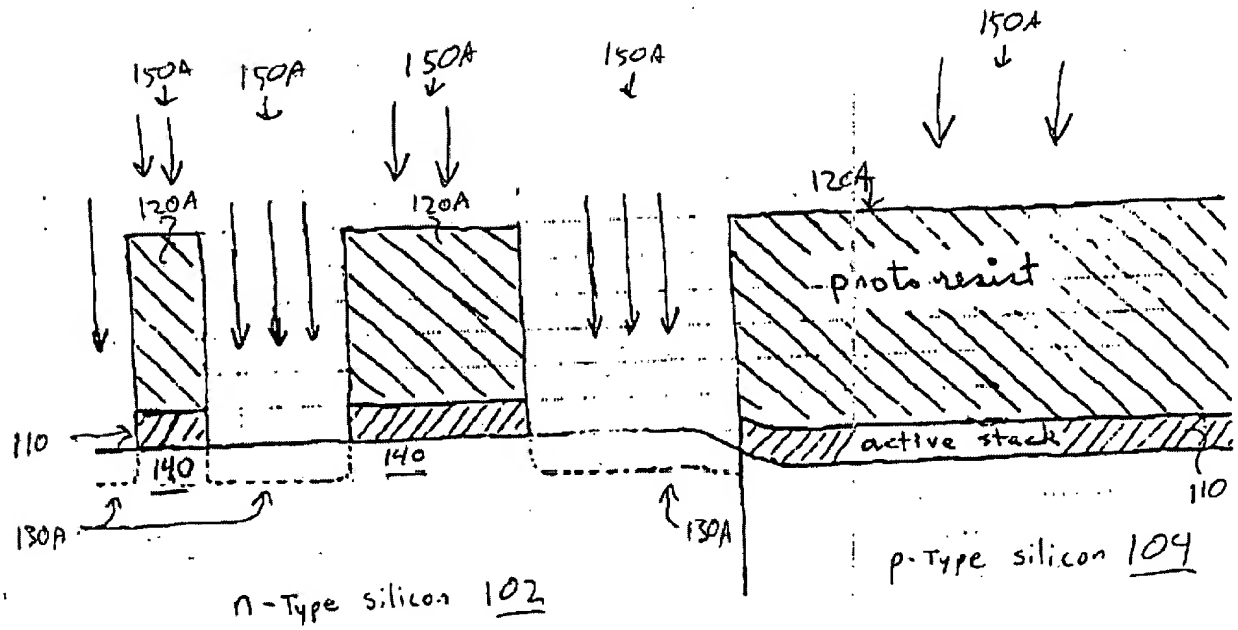

Fig. 1

Specification, Figure 1, page 7, lines 10–15. A photoresist 120A is formed and patterned with openings therethrough over isolation areas 130A within the n region 102, with the patterned photoresist 120A being used to mask both (a) etching of the oxidation barrier 110 to expose the isolation areas 130A within n region 102 and to form an "active stack" that will be employed as part of the gate electrodes for devices in the n region 102 and (b) implantation of a channel stop into those isolation areas 130A. Specification, page 7, lines 16–25.

The patterned photoresist 120A is then stripped and a second patterned photoresist 120B is formed with openings over isolation areas 130B within the p region 104:

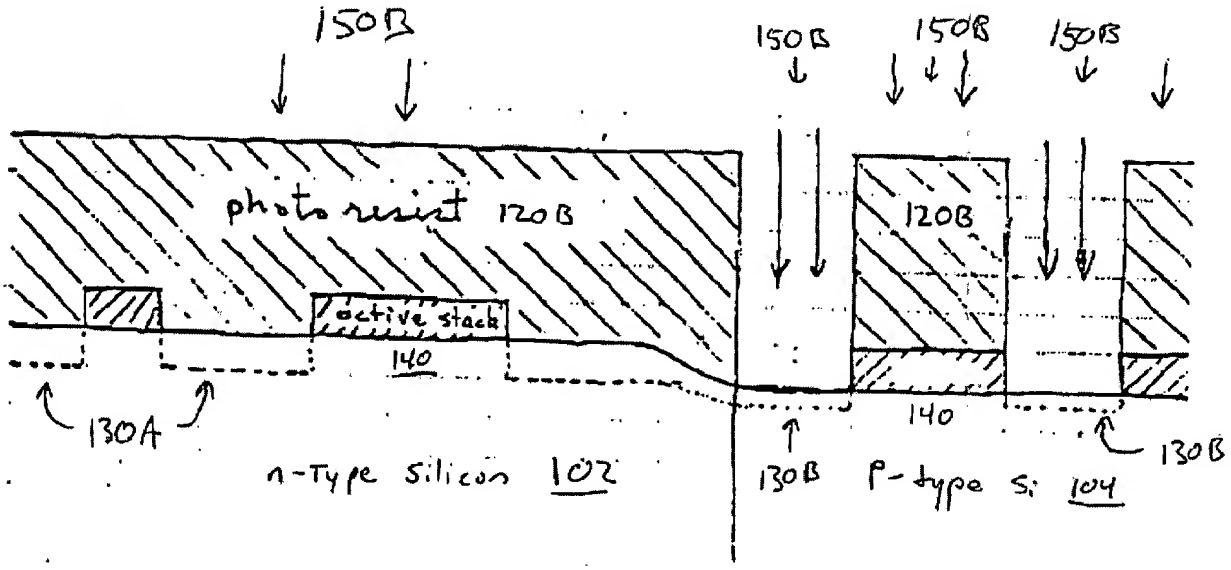

Fig. 2

Specification, Figure 2, page 8, lines 1–5. As with the first patterned photoresist 120A, the second patterned photoresist 120B is used to mask both (a) etching of the oxidation barrier 110 to expose the isolation areas 130B within p region 104 and form an active stack for gate electrodes of devices in the p region 104 and (b) implantation of a channel stop into those isolation areas 130B. Specification, page 8, lines 6–13. It should be noted that the second patterned photoresist 120B is formed directly on the isolation areas 130A and the patterned active stack 110 in n region 102. While prior art processes might grow an isolation oxide over the isolation areas 130A in n region

before patterning the oxidation barrier and performing a channel stop implant in p region 104, the present invention defers such oxidation until after the oxidation barrier 110 over both the n and p regions 102 and 104 has been patterned, and channel stops have been implanted in the isolation areas 130A and 130B in both n and p regions 102 and 104. Specification, page 8, lines 18–21.

STATUS OF CLAIMS

Claims 1 and 32–47 are pending in the present application. Claims 46–47 were withdrawn. Claims 1 and 32–45 were rejected under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement. The rejection of pending claims 1 and 32–45 is appealed.

STATUS OF AMENDMENTS

An Advisory Action mailed March 2, 2004 refused entry of the amendment to the claims filed February 4, 2004 following the final Office Action mailed December 3, 2003 in this matter on the grounds that the amendments raised new issues requiring further search and consideration.

ISSUES ON APPEAL

Claims 1 and 32–45 were rejected under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement. The sole issue on appeal is whether claims 1 and 32–45 were properly rejected under 35 U.S.C. § 112, first paragraph.

GROUPING OF CLAIMS

Claims 1 and 32–45 were rejected under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement. For purposes of this appeal, the pending claims will be grouped together.

ARGUMENT

Claims 1 and 32–45 were rejected under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement. Specifically, independent claim 1 recites: "without forming an oxide on the first isolation areas, forming a second patterned layer which exposes second isolation areas in the p-type region and which covers substantially all of the n-type region and active device areas in the p-type region." Similarly, independent claim 38 recites: "without growing an oxide on isolation regions within the first well, patterning the active stack using a second patterned layer to expose isolation regions within the second well having a second conductivity type." The underlined portion of the two limitations forms the basis of the written description rejection.

To satisfy the written description requirement of 35 U.S.C. § 112, first paragraph, a patent specification must describe the claimed invention in sufficient detail that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention. MPEP §§ 2163, 2163.02, pp. 2100-159, 2100-171 (8th ed. rev. 1 February 2003). The requisite description may be made through words, drawings and/or formulas. *Id.* The subject matter of the claim need not be

described literally (i.e., using the same terms or *in haec verba*) in order for the disclosure to satisfy the description requirement. MPEP § 2163.02, p. 2100-172. Compliance with the written description requirement is evaluated based on the specification and drawings as a whole. MPEP § 2163, p. 2100-163. The Patent Office has the initial burden of presenting evidence or reasons why a person skilled in the art would not recognize that the written description of the invention provides support for the claims. MPEP § 2163, p. 2100-163.

The final rejection in the instant application contains simply a naked assertion that the specification fails to satisfy the written description requirement with respect to forming a second patterned layer exposing second isolation areas without forming an oxide on the first isolation areas as recited in the claims:

> Claims 1 and 38 recite, ". . . without forming an oxide on the first isolation areas, forming a second patterning layer . . .". However, there is no description of forming a second patterning layer "without forming an oxide" as recited.

Paper No. 11212003, page 2. No evidence or reasons why a skilled artisan would not recognize that the inventor possessed the claimed subject matter at the time the application was filed were provided.

As noted above, the specification describes forming and patterning of the second photoresist 120B covering at least the whole n region 102. Specification, page 8, lines 2–5. In particular, the second photoresist 120B ("second patterned layer which exposes second isolation areas in the p-type region . . .") is depicted in Figure 2 as being formed directly on the isolation areas 130A ("first isolation areas") in the n region 104. Specification, Figure 2. No oxide is described as being formed

on isolation areas 130A prior to formation of second photoresist 120B, nor is any oxide depicted as being formed on isolation areas 130A prior to formation of second photoresist 120B and/or between isolation areas 130A and second photoresist 120B. The specification teaches that the isolation or "field" oxide is grown on the isolation areas 130A and 130B after the oxidation barrier 110 is patterned over both the n and p regions 102 and 104 (and channel stops are implanted into both isolation regions 130A and 130B). Specification, page 4, lines 5–7 and page 8, lines 12–19. Accordingly, a skilled artisan would recognize without difficulty from the text and drawings as filed that the Applicant had possession of the claimed invention at the time the application was filed.

CONCLUSION

The specification and drawings as filed contain adequate written description of the claimed invention. Therefore, the rejection under 35 U.S.C. § 112, first paragraph is improper. Applicant respectfully requests that the Board of Appeals reverse the decision of the Examiner below rejecting pending claims 1 and 32–45 in this application.

Respectfully submitted,

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Date: 6-8-04

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CLAIMS ON APPEAL

1. An integrated circuit structure fabrication method, comprising:

forming n-type and p-type regions within a substrate;

forming an oxidation barrier on a surface of the substrate over the n-type and p-type regions;

forming a first patterned layer which exposes first isolation areas in the n-type region and which covers substantially all of the p-type region and active device areas in the n-type region;

removing portions of the oxidation barrier layer exposed by the first patterned layer to expose the first isolation areas;

implanting a first channel-stop dopant into the first isolation areas exposed by the first patterned layer and the oxidation barrier layer;

removing the first patterned layer;

without forming an oxide on the first isolation areas, forming a second patterned layer which exposes second isolation areas in the p-type region and which covers substantially all of the n-type region and active device areas in the p-type region;

removing portions of the oxidation barrier layer exposed by the second patterned layer to expose the second isolation areas;

implanting a second channel-stop dopant into the second isolation areas exposed by the second patterned layer and the oxidation barrier layer;

removing the second patterned layer; and

growing a field oxide on the first and second isolation areas where exposed by the oxidation barrier layer in a single oxidation step.

32. The method of claim 1, wherein the first isolation areas are protected by only the second patterned layer during implantation of the second channel-stop dopant into the second isolation areas.

33. The method of claim 1, wherein the oxidation barrier overlies an oxide layer which is patterned together with the oxidation barrier using the first and second patterned layers to expose the first and second isolation areas.

34. The method of claim 33, wherein the oxidation barrier overlies a polysilicon layer on the oxide layer which is patterned together with the oxidation barrier and the oxide layer using the first and second patterned layers to expose the first and second isolation areas.

35. The method of claim 1, wherein critical dimensions for the active device areas in the p-type region are selected independently from critical dimensions selected for the active device areas in the p-type region.

36. The method of claim 1, further comprising:

prior to removing the first patterned layer, etching the substrate through the first patterned layer to form recesses in the first isolation areas in the n-type region.

37. The method of claim 1, further comprising:

prior to removing the second patterned layer, etching the substrate through the second patterned layer to form recesses in the second isolation areas in the p-type region.

38. A method of forming an integrated circuit structure, comprising:

forming an active stack over two adjacent wells having opposite conductivity types within a substrate;

patterning the active stack using a first patterned layer to expose isolation regions within a first well having a first conductivity type;

implanting a channel-stop into the exposed isolation regions within the first well masked by the first patterned layer, wherein the first patterned layer protects active device areas in the first well and substantially all of the second well during the implant of the channel-stop in the exposed isolation regions within the first well;

removing the first patterned layer;

without growing an oxide on isolation regions within the first well, patterning the active stack using a second patterned layer to expose isolation regions within the second well having a second conductivity type;

implanting a channel-stop into the exposed isolation regions within the second well masked by the second patterned layer, wherein the second patterned layer protects active device areas in the second well and substantially all of the first well during the implant of the channel-stop in the exposed isolation regions within the second well;

removing the second patterned layer; and

growing a field oxide on the isolation regions within both the first and second wells with a

single oxidation step.

39. The method of claim 38, wherein the isolation regions within the first well are protected by only the second patterned layer during implantation of the channel-stop into the isolation regions within the second well.

40. The method of claim 38, wherein the active stack further comprises:

a nitride layer overlying an oxide layer, wherein the nitride and oxide layers are patterned together using the first and second patterned layers to expose the first and second isolation areas.

41. The method of claim 40, wherein the active stack further comprises:

a polysilicon layer between the nitride and oxide layers, wherein the polysilicon layer is patterned together with the nitride and oxide layers using the first and second patterned layers to expose the first and second isolation areas.

42. The method of claim 38, wherein critical dimensions for the active device areas in the first well are selected independently from critical dimensions selected for the active device areas in the second well.

43. The method of claim 38, further comprising:

prior to removing the first patterned layer, etching the substrate through the first patterned layer to form recesses in the exposed isolation regions within the first well.

44. The method of claim 38, further comprising:

prior to removing the second patterned layer, etching the substrate through the second patterned layer to form recesses in the exposed isolation regions within the second well.

45. The method of claim 38, wherein the first well is an n-well and the second well is a p-well.

46. An integrated circuit structure, comprising:

an active stack over two adjacent wells having opposite conductivity types within a substrate,

wherein the active stack has openings therethrough over isolation regions within a first well having a first conductivity type and over isolation regions within the second well having a second conductivity type;

a channel-stop within the substrate beneath the isolation regions within the first well; and

a patterned masking layer on the active stack and directly on the substrate within the isolation regions within the first well, wherein the patterned masking layer has openings therethrough over the isolation regions within the second well.

47. The integrated circuit structure of claim 45, further comprising:

a channel-stop within the substrate beneath the isolation regions within the second well.